

109201-2/594001

Interconnect Fabric Module

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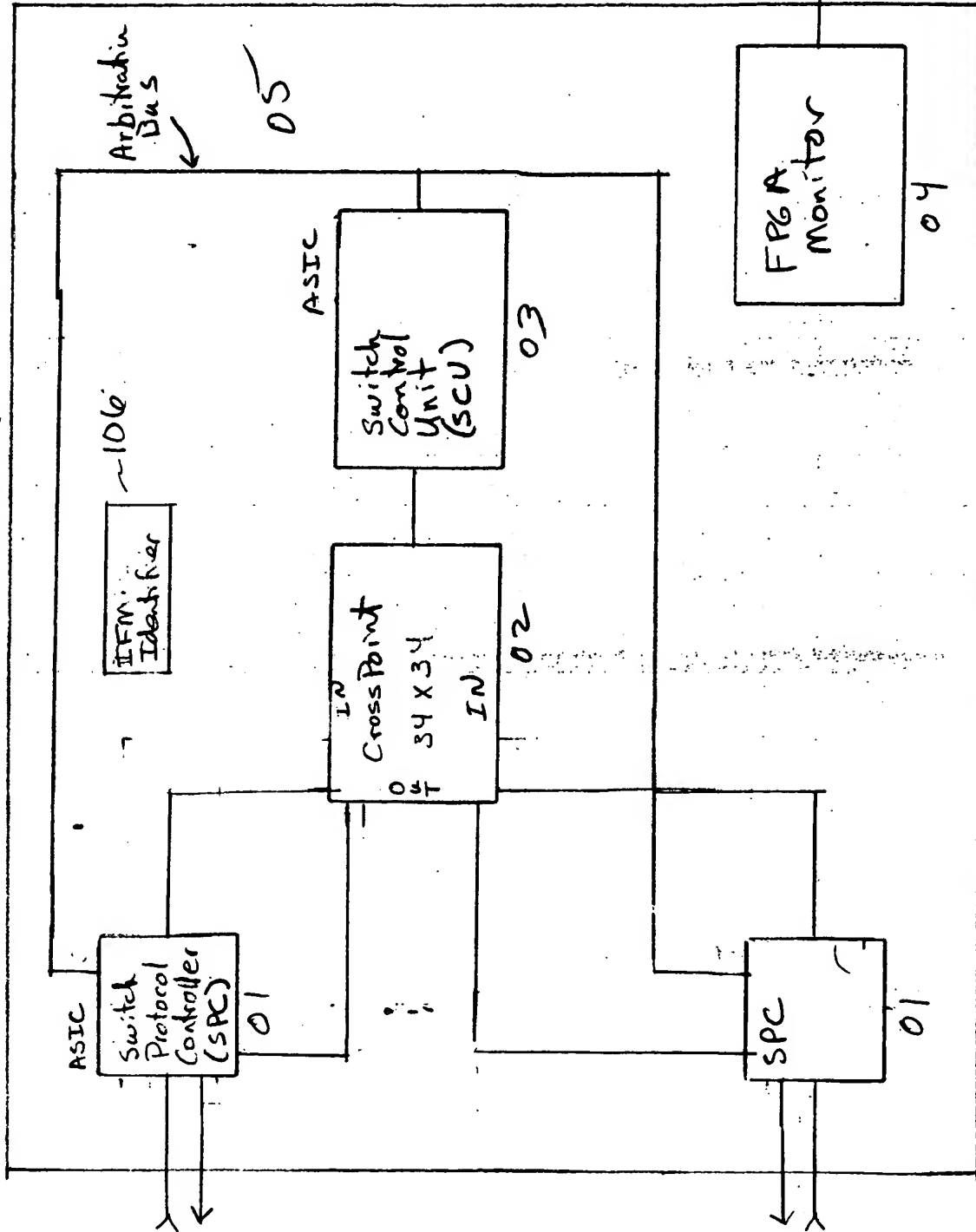


Fig 1

FO9201"27594001

Switch Protocol Controller (SPC) Arbitration Bus

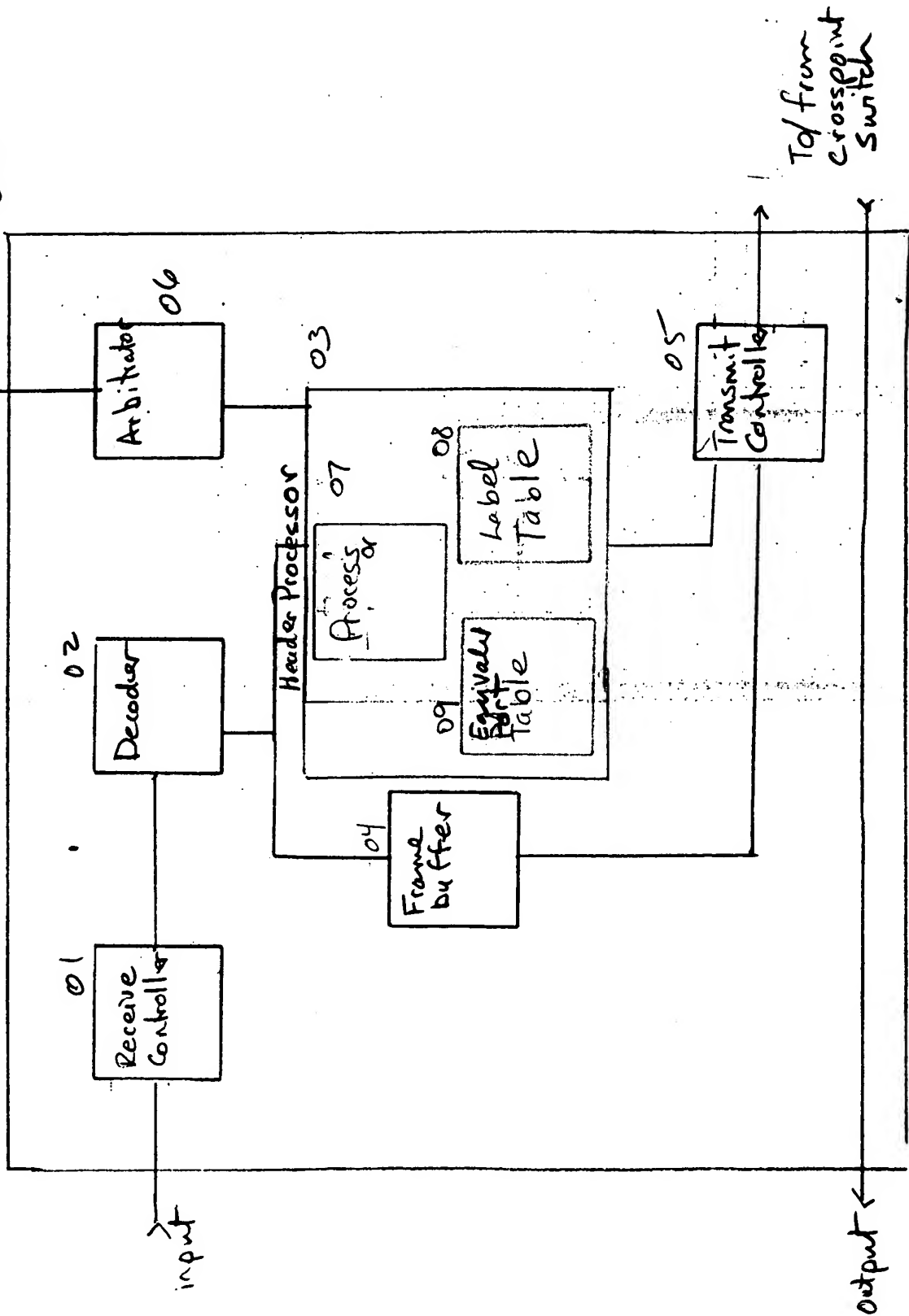
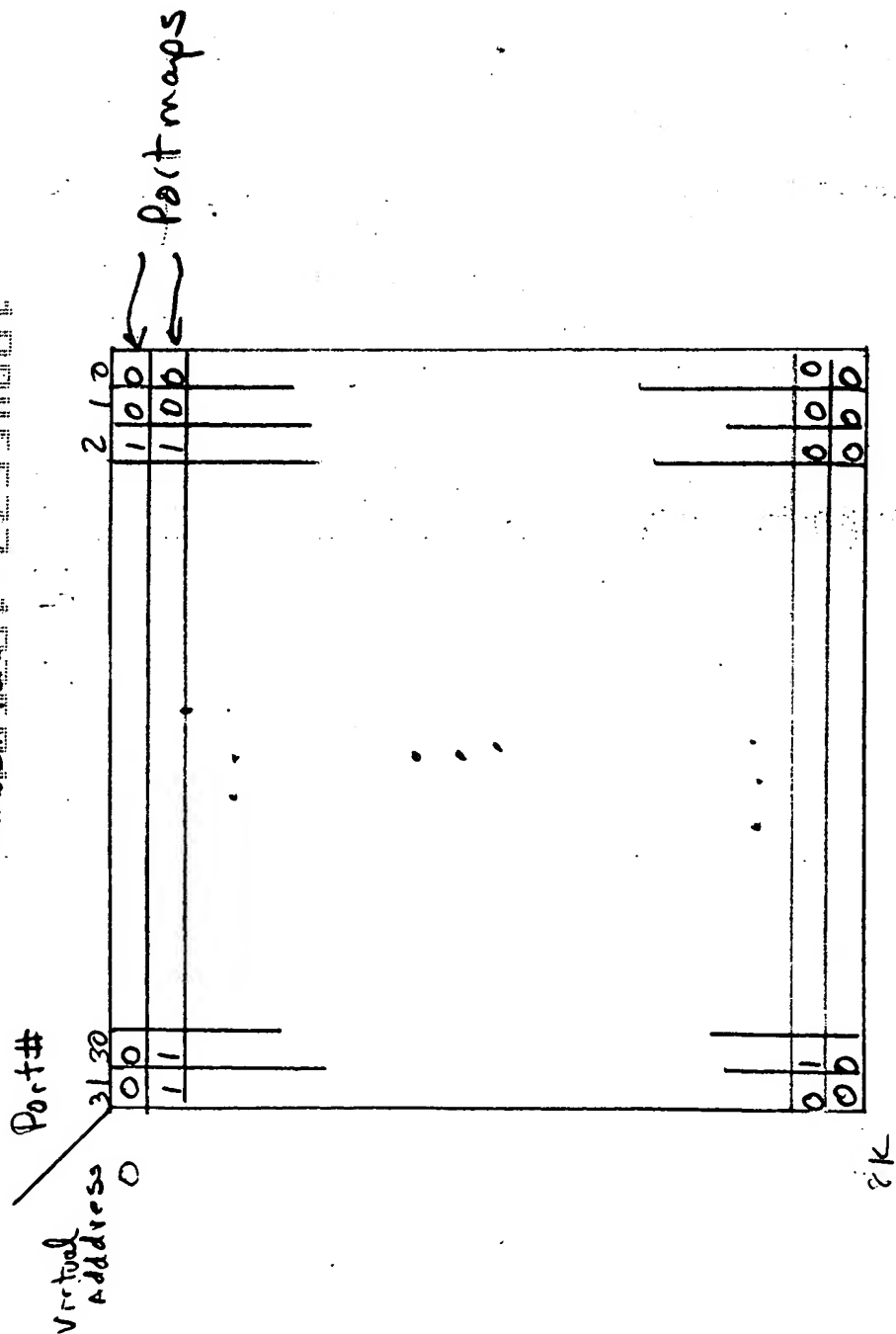


Fig 2

Label: Table "2004001"



M
ص
L

1045400F 259400F 20920F

Frame

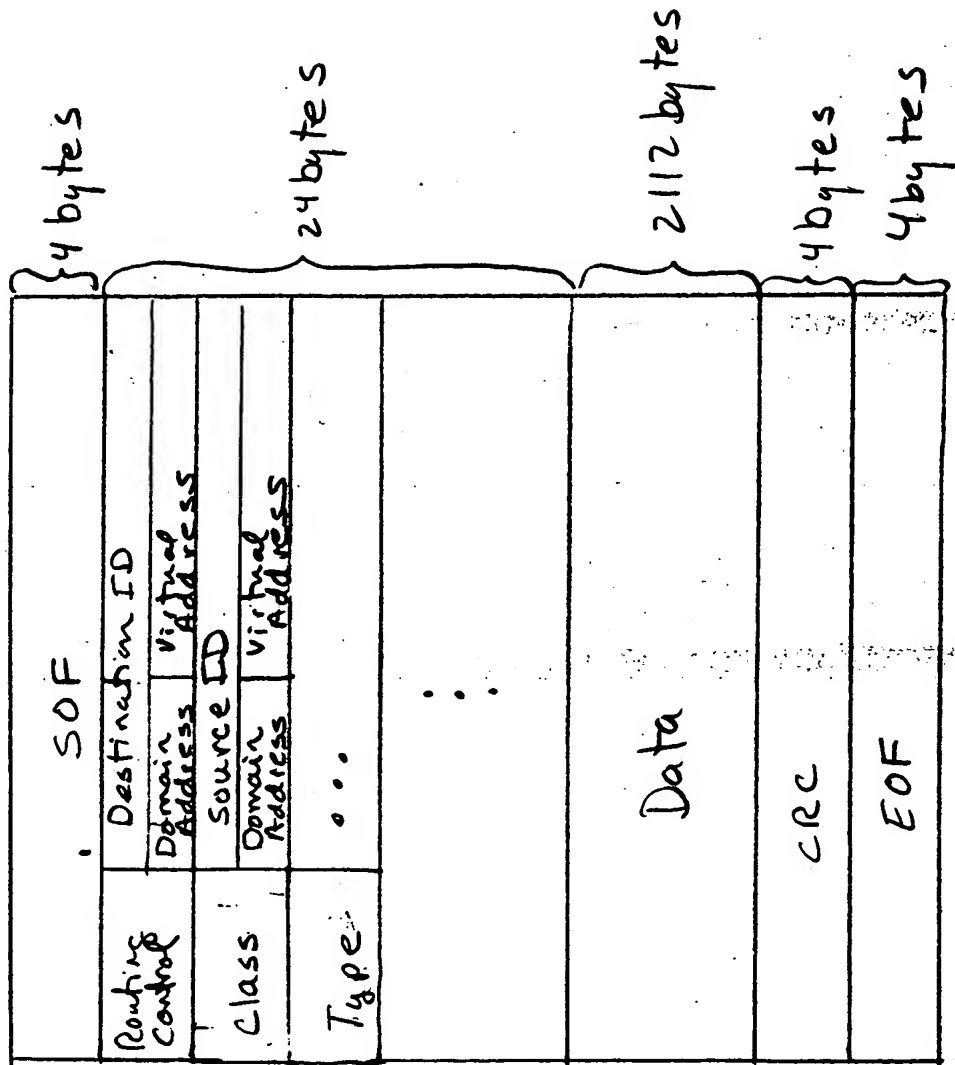


Fig 4

10046572.102601

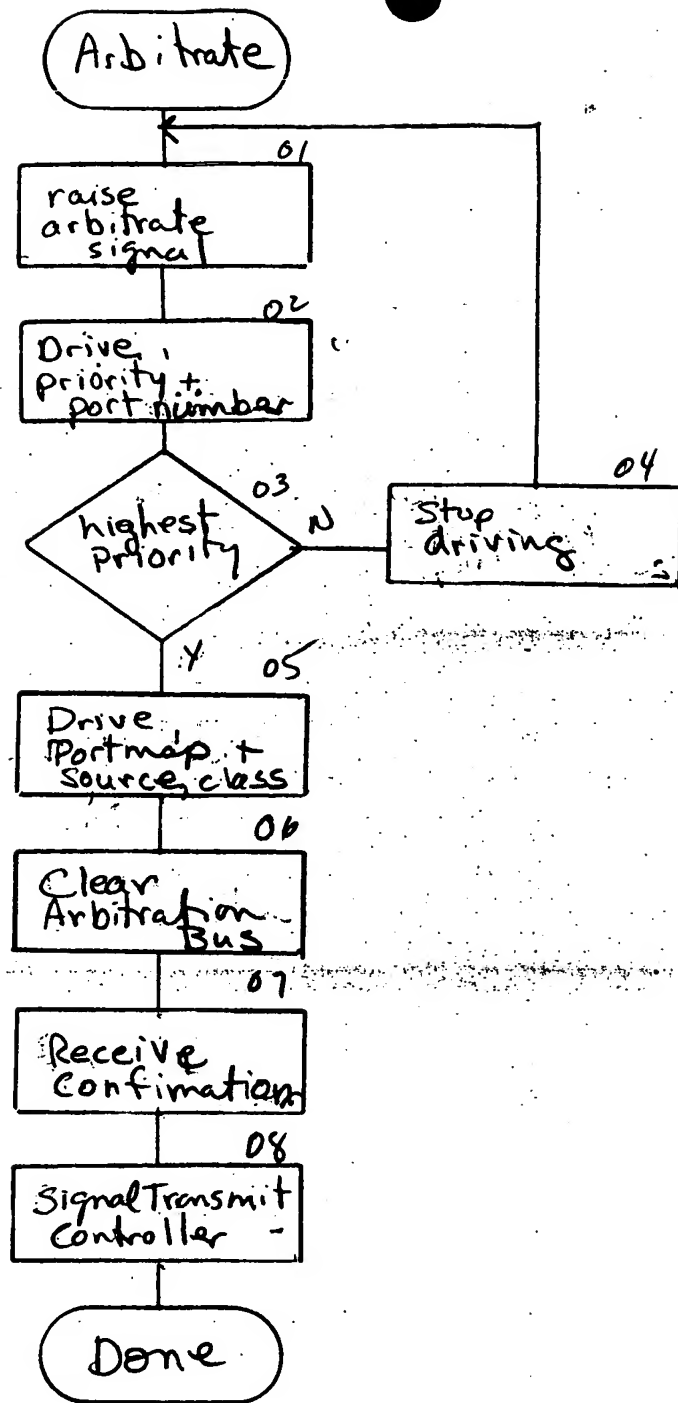


Fig 5

Transmission Controller

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graph LR; A[Frame Header Processor] --> B[Frame Generator]; B --> C[Multiplexer]; D[Frame Buffer] --> C; C --> E[Encoder]; E --> F[to cross point];
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The diagram illustrates the data flow in a video encoding system. It starts with a 'Frame Header Processor' which sends data to a 'Frame Generator'. The 'Frame Generator' then sends data to a 'Multiplexer'. A 'Frame Buffer' also feeds into the 'Multiplexer'. The output of the 'Multiplexer' goes to an 'Encoder', which finally sends the signal 'to cross point'.

4.8

109201-22594001

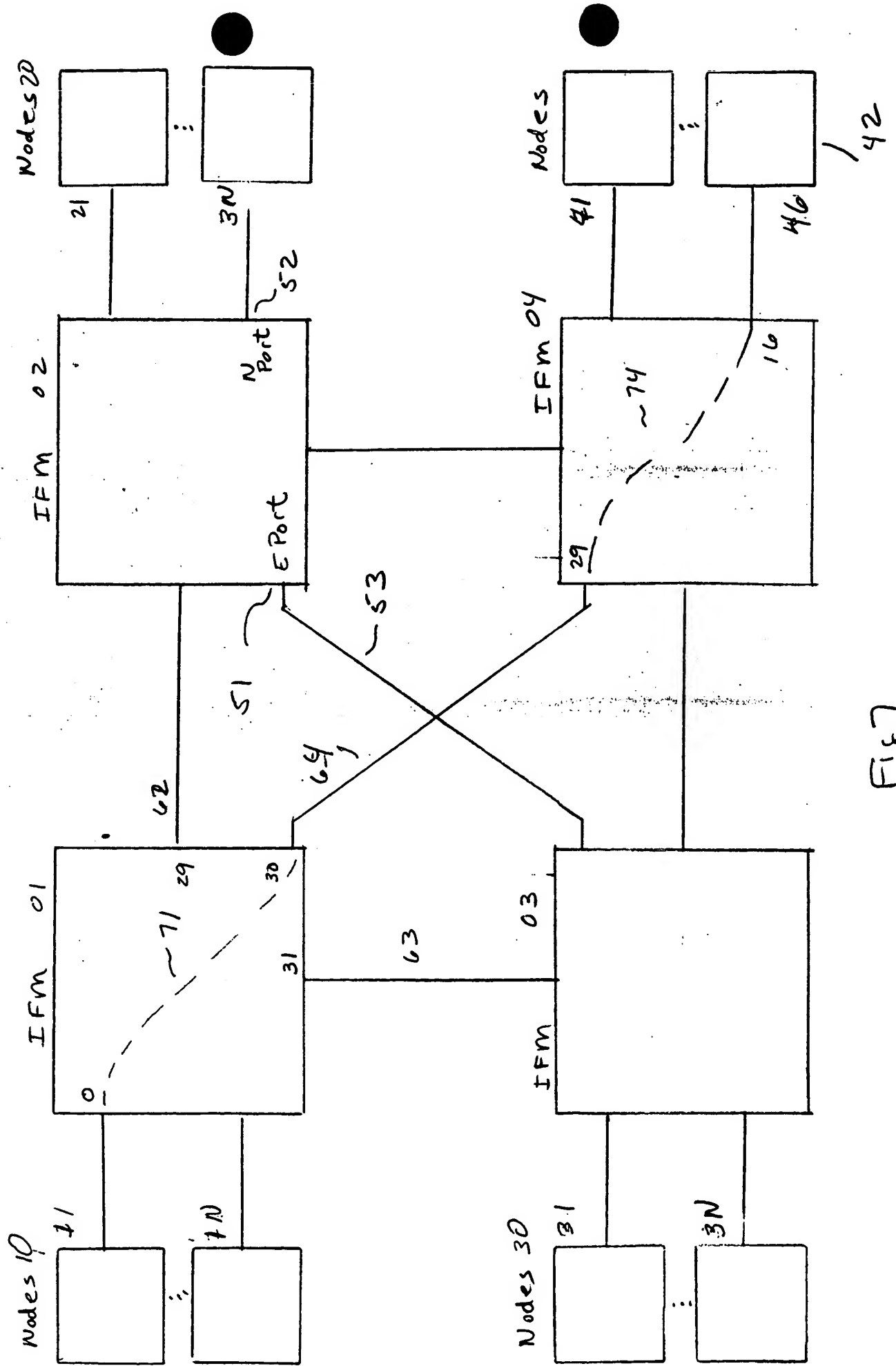


Fig 7

FO920T 2259400T

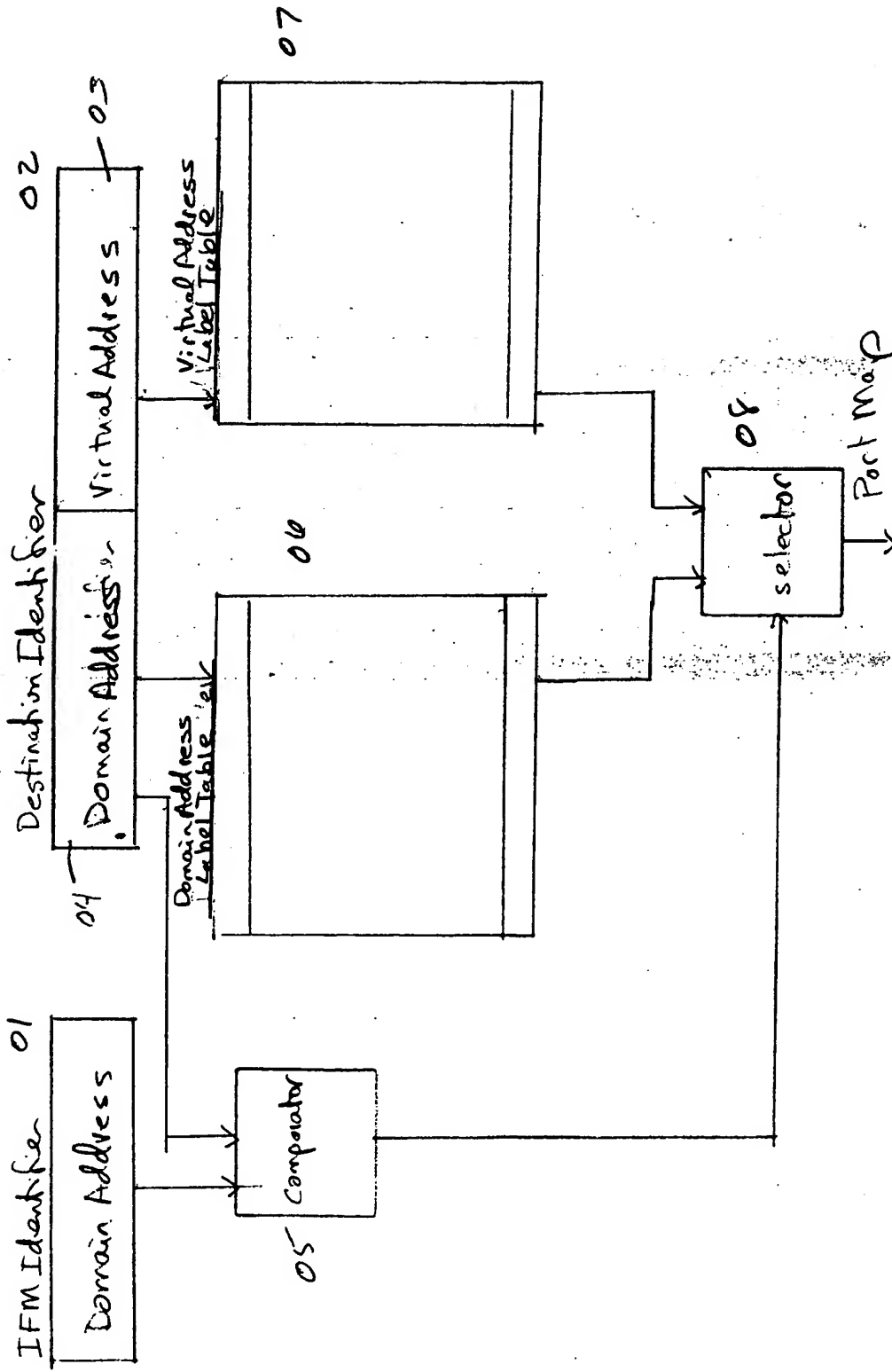


Fig. 8

10920T-2259400T

Quad Switch Protocol Controller

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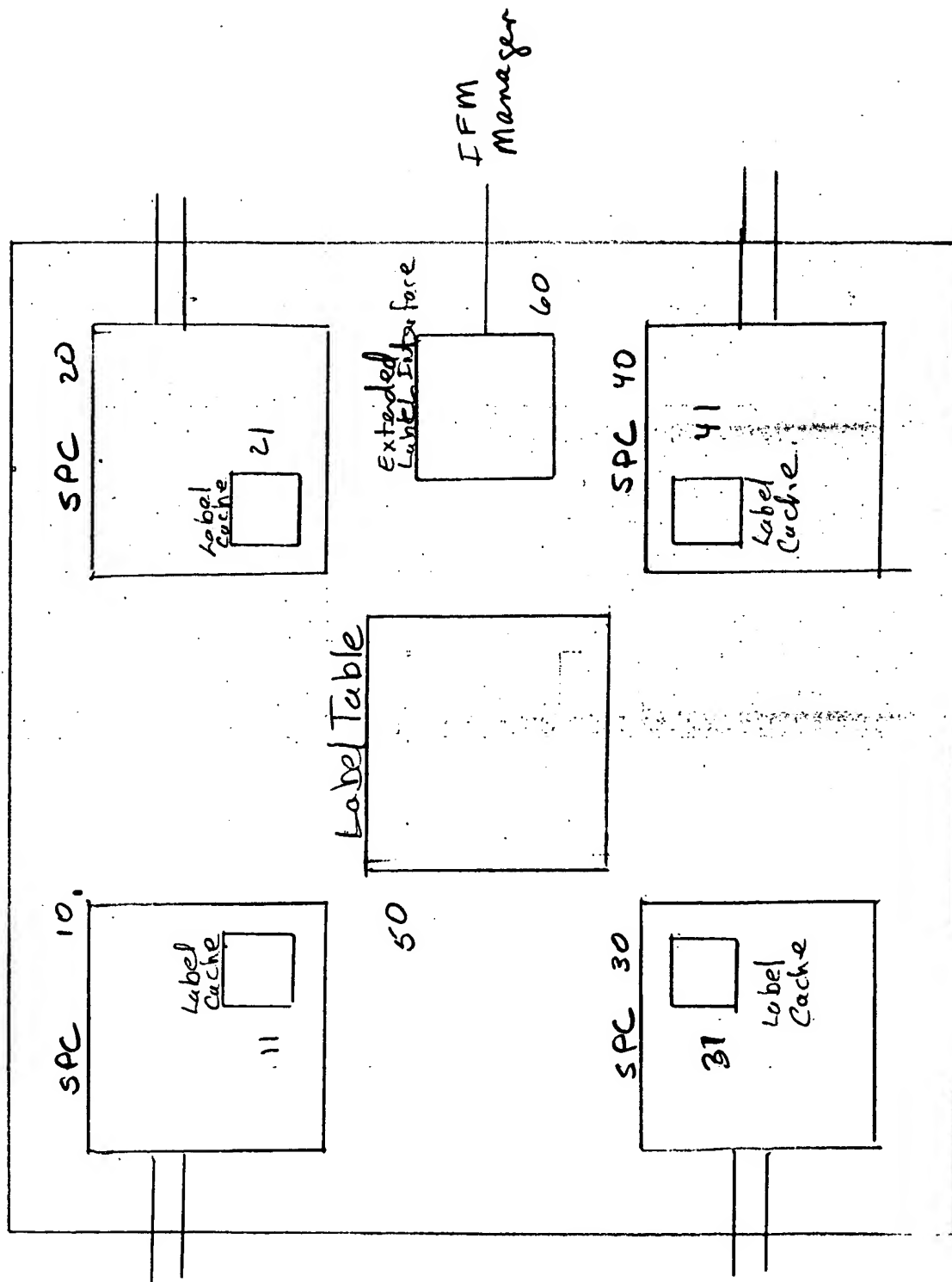


Fig 9

109201-259400

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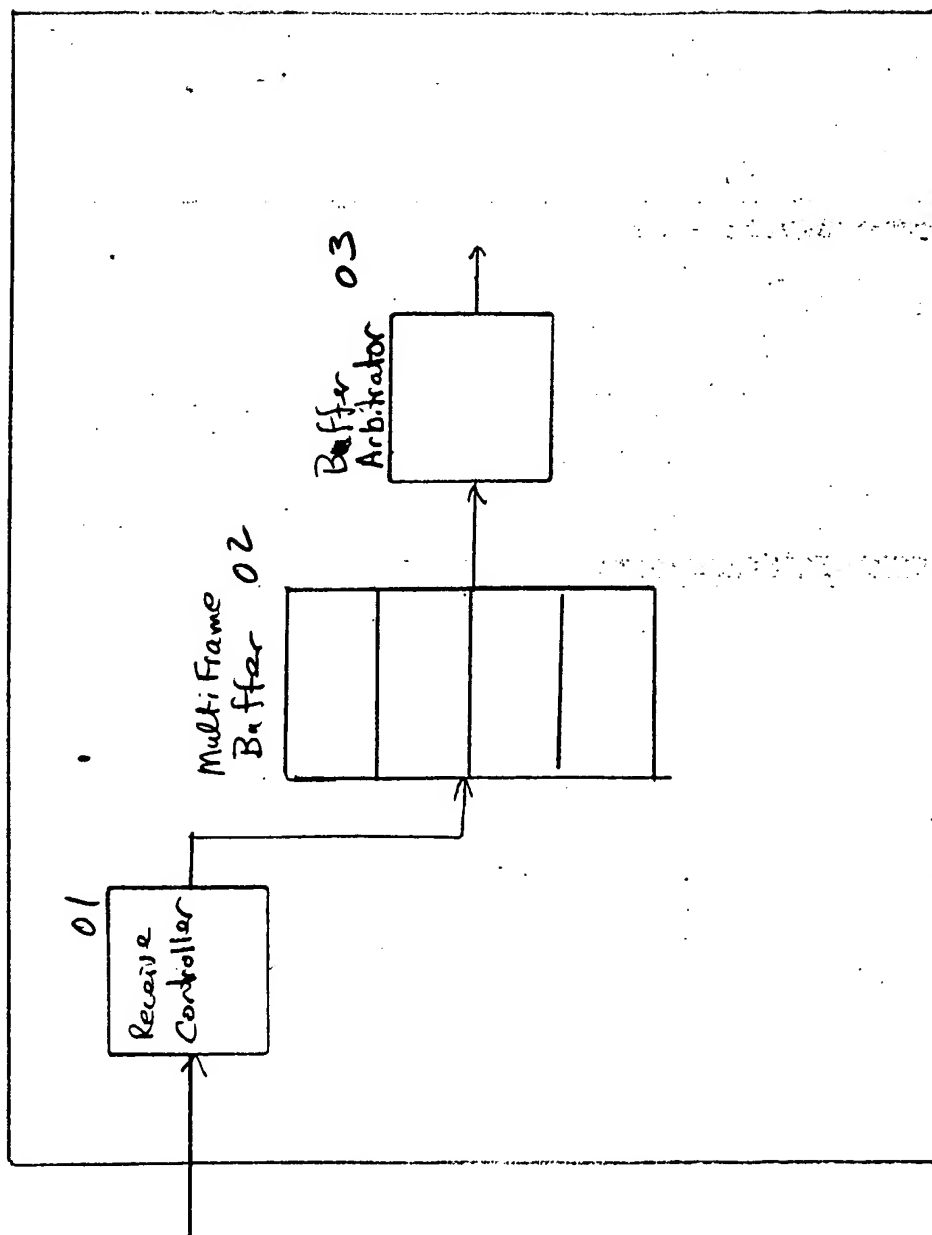


Fig 10

10046572.102601

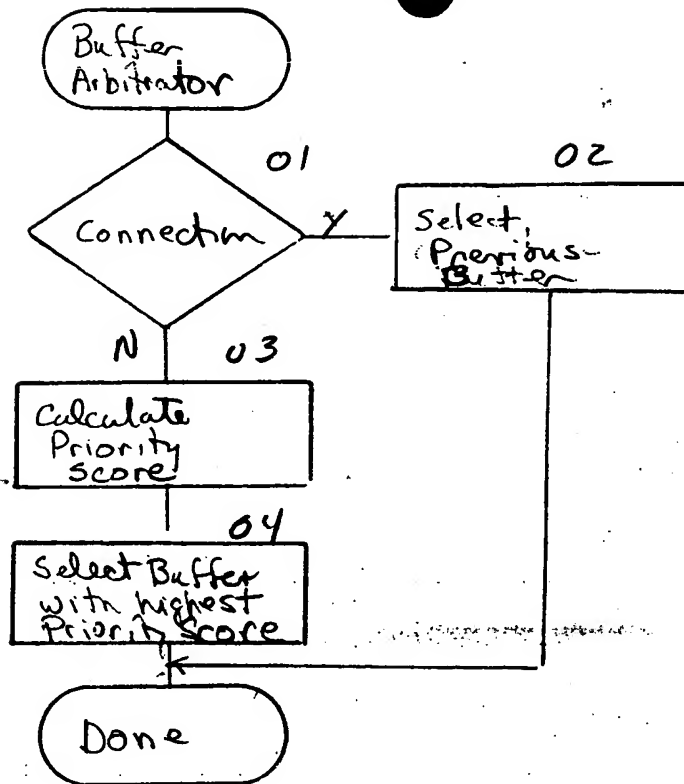


Fig 11

10046572-102601

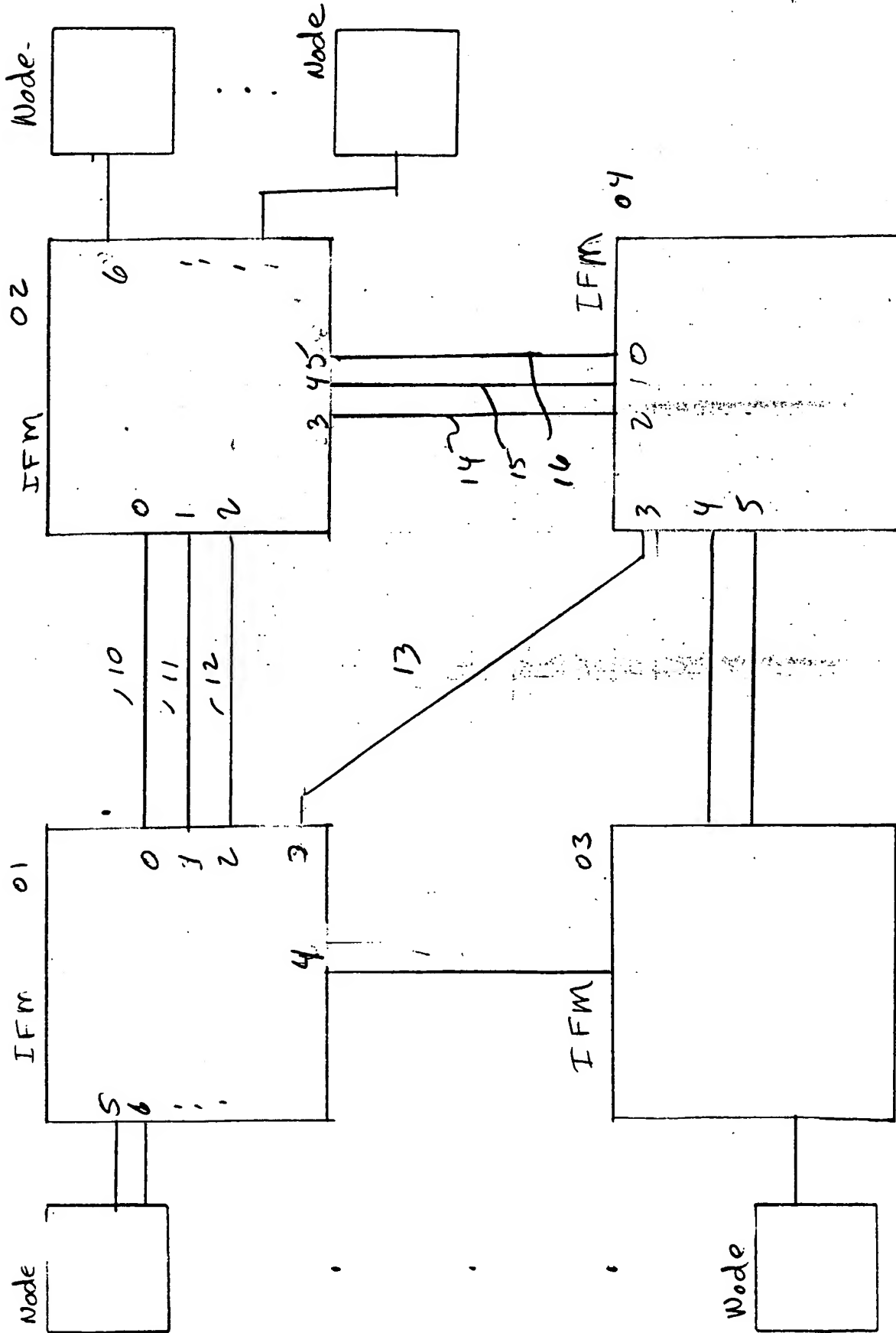


Fig 12

1004557-1060

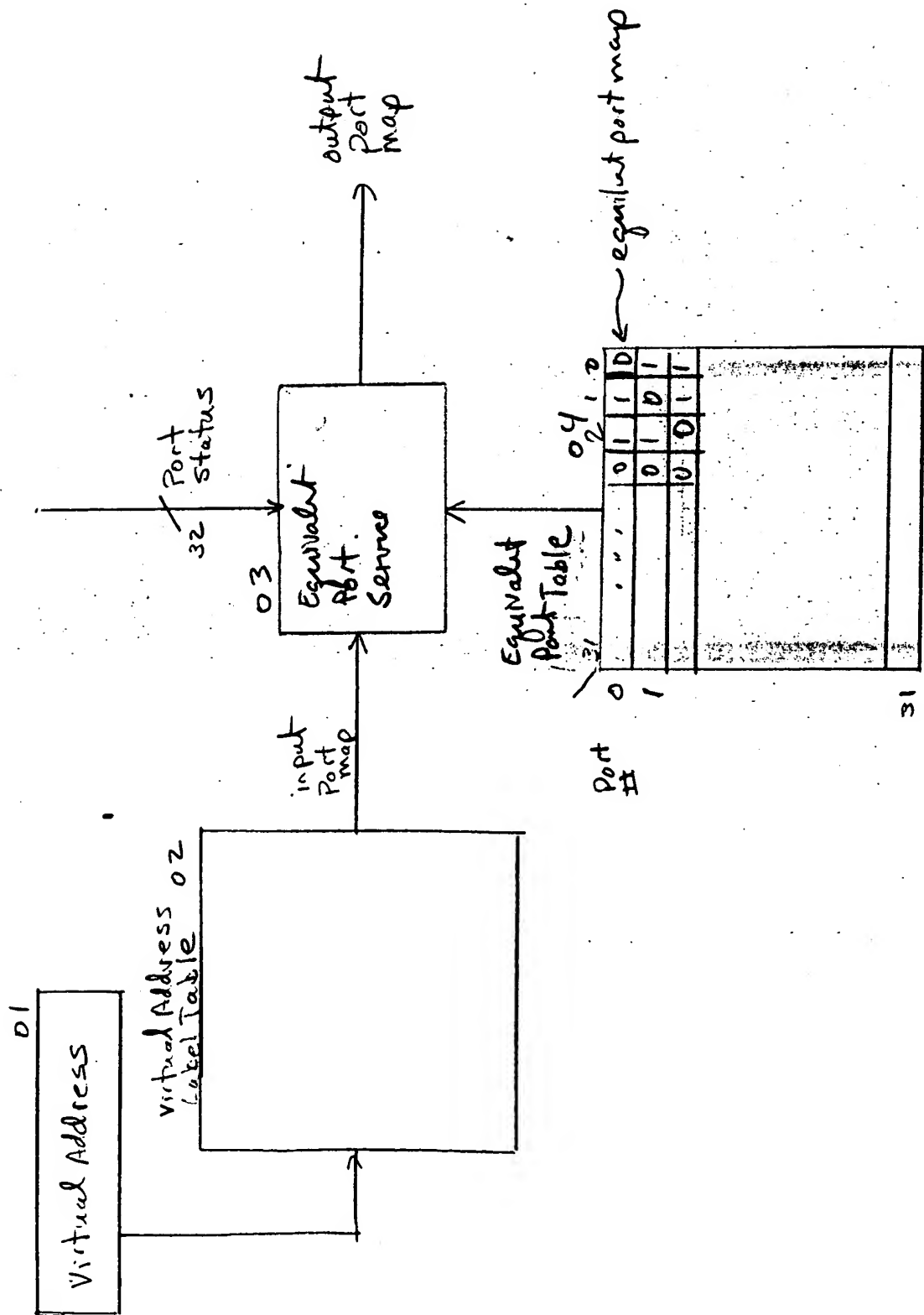


Fig 13

10046572-102601

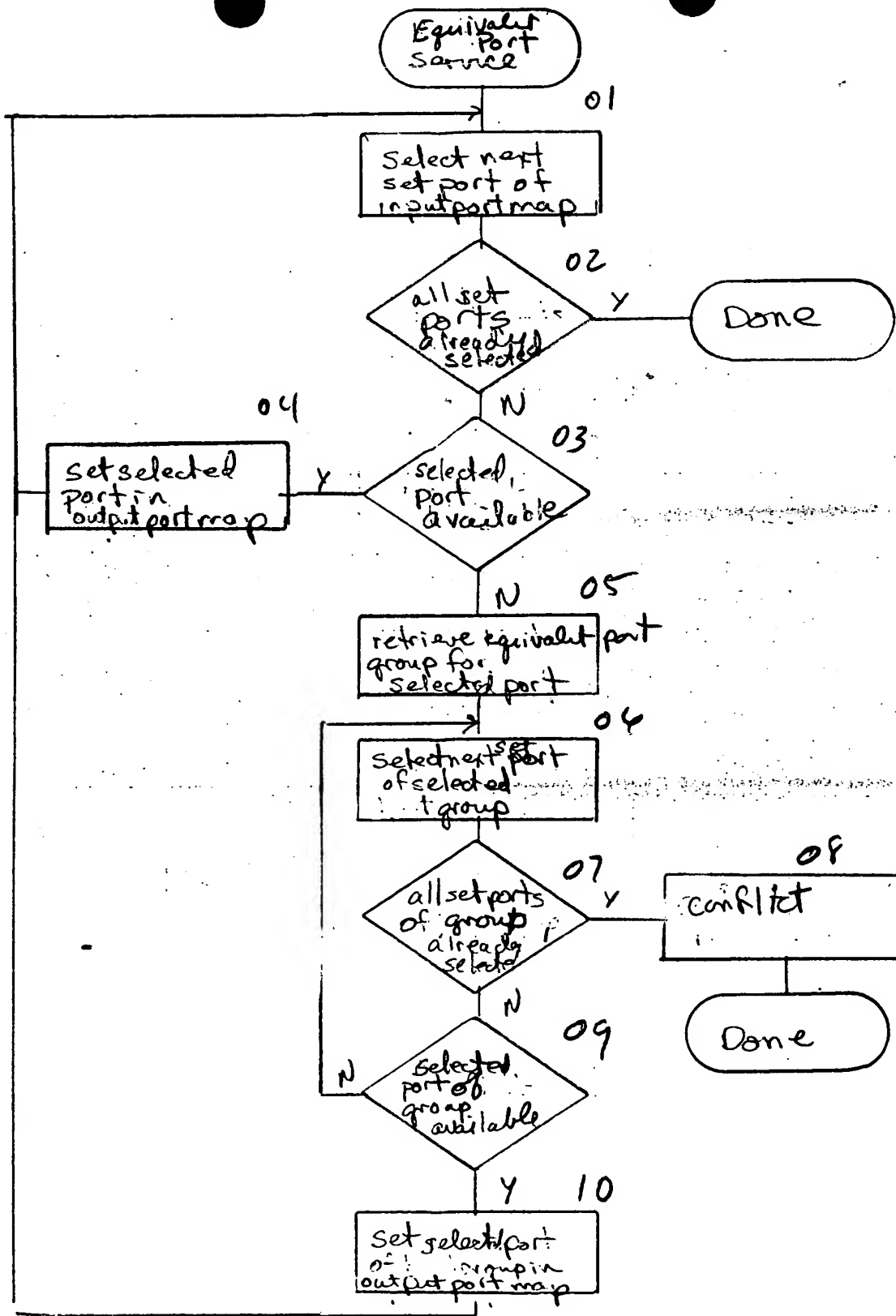


Fig 14

10920T-2459400F

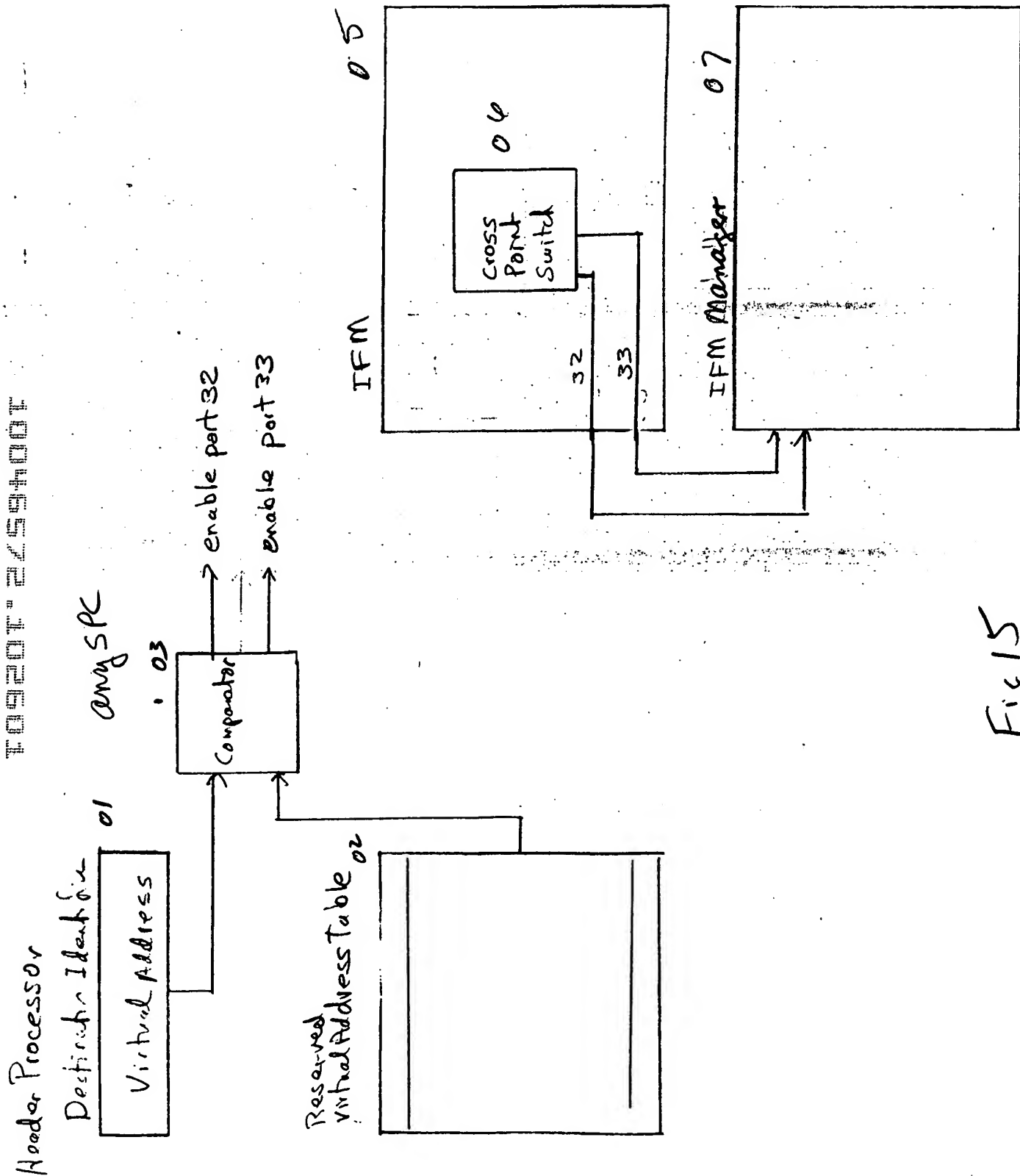
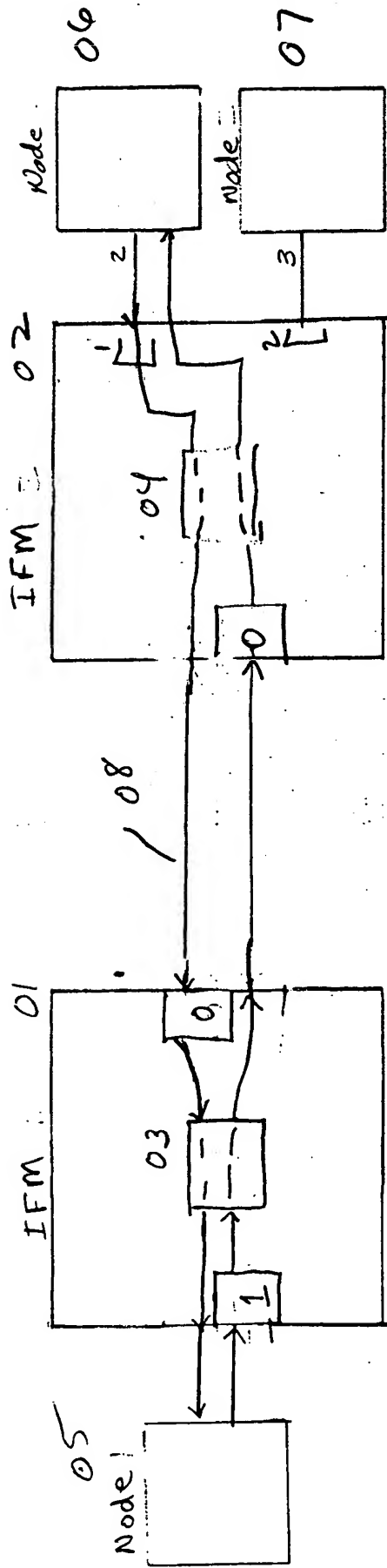


Fig 15



Dead lock

10

Time Node 1605 IFM 1601 Node 1606 IFM 1602

0	Send start connect	Send start connect	
1	Connect 1 ↔ 0	Connect 2 ↔ 0	
2	Forward start connect	Forward start connect	
3	Can't forward start connect Node 1	Can't forward start connect	

Fig 16

When end-to-end
not established

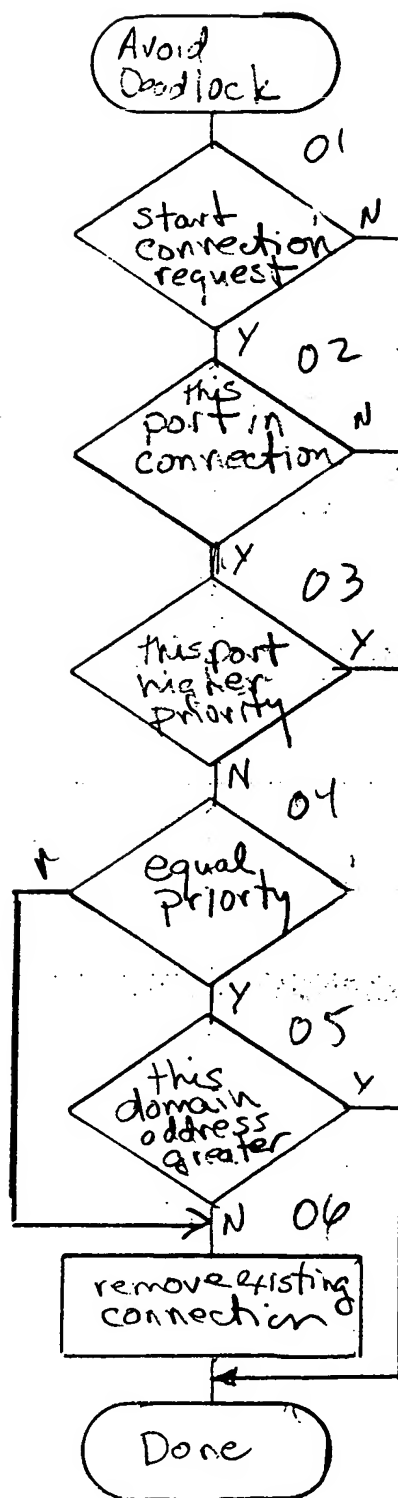


Fig 17

10046572-102601

10046572-102604

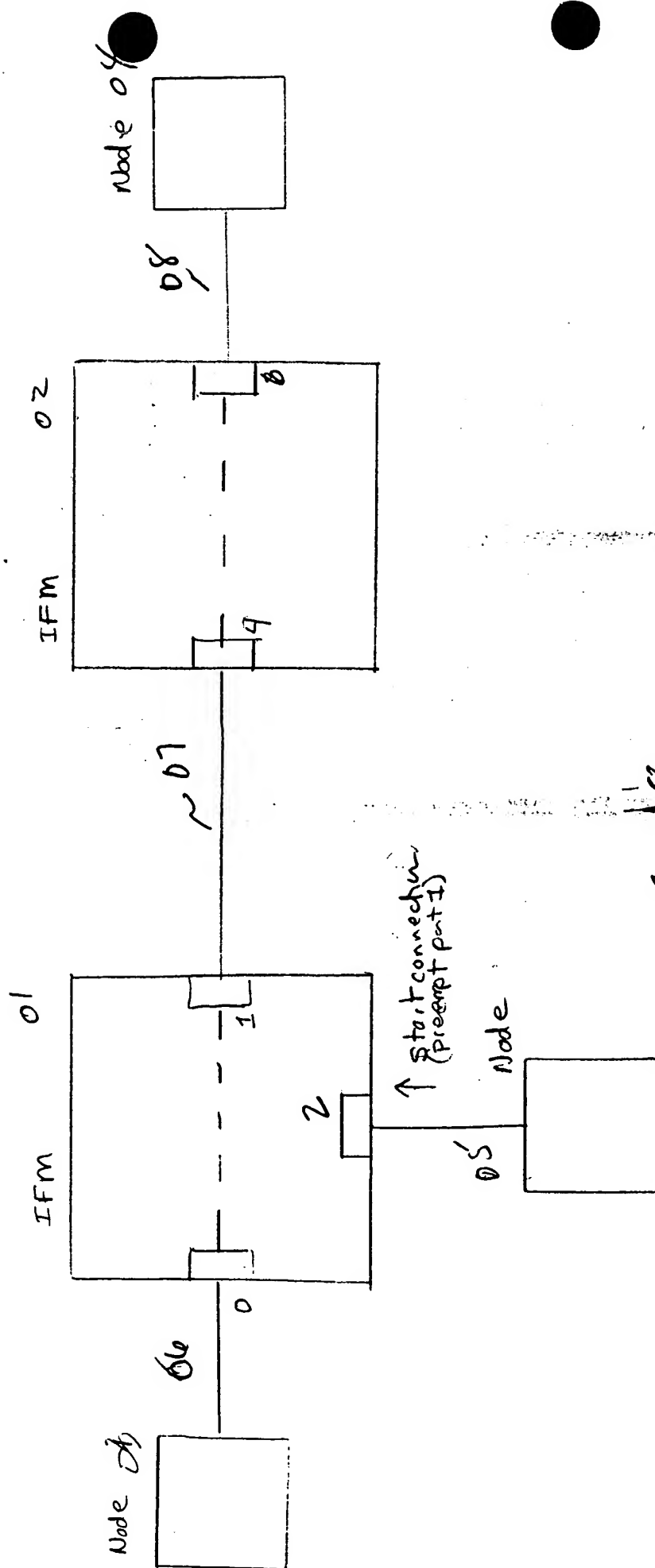


Fig 18

input port

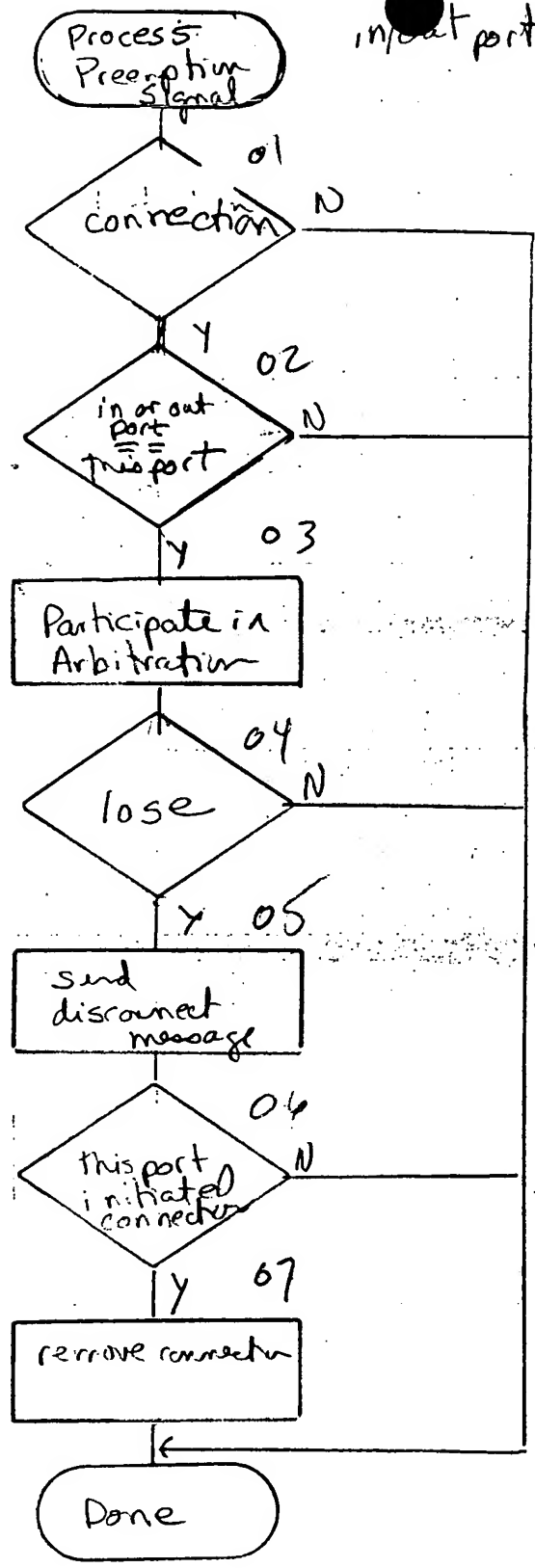


Fig. 19

10046572-102601

10046572-102601

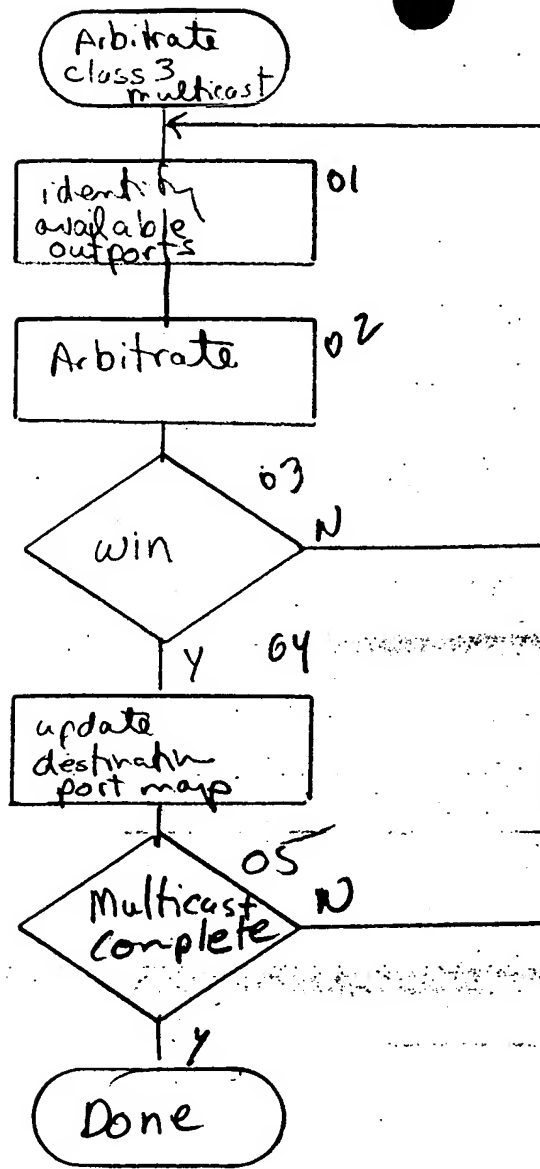


Figure 20